picture data, and for inverting a polarity of the analog output of said D/A converter according to the signal polarity inversion signal,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction.

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REMARKS

Claims 1, 2, 4, 5, 7-19, 21, 22 and 24-48 are now presented for examination. Claims 1, 18, 38 and 43 are the only independent claims. Claims 18, 38 and 43 have been amended to define still more clearly what Applicants regard as their invention.

Claims 1-5, 7-12, 15, 16, 18-22, 24-29, 32, 33, 35 and 38-47 were rejected under 35 U.S.C. § 103 as obvious from Lewis in view of Yamaguchi and Shinya. Claims 13, 14, 17, 30, 31, 34, 36, 37 and 48 were rejected under 35 U.S.C. § 103 as obvious from Lewis in view of Yamaguchi and Shinya and further in view of Misawa. The Examiner's bases for the rejection is set forth in detail from pages 2-15 of the Office Action.

Applicants respectfully traverse the rejections, and submit that the independent Claims 1, 18, 38 and 43, together with the remaining claims dependent thereon, are patently distinct from the cited prior art for at least the following reasons.

I. The References Do Not Teach all of the Features of Claim 1.

Claim 1 recites that digital picture signals from the horizontal scanning circuit are transferred to the latch circuit and subsequently to the D/A converter for

converting the picture signals into analog signals. Circuitry in combination with the D/A converter allows for inverting the polarity of the analog signal from the D/A converter. Signal inversion is exercised prior to or in concert with the D/A converter. The inverted analog signal from the D/A converter is then written into the liquid crystal picture elements through the buffer. By virtue of this recited structure, the transfer of the picture signals is conducted in a digital manner just before the D/A converters, signal quality is maintained irrespective of decay of the signal and improved picture quality is realized without influence of noises.

Lewis shows a display driver architecture using D/A converters. Yamaguchi is relied upon as showing inverting analog signal polarity. Shinya is relied upon as showing the buffering of the analog signal. However, a combination of Lewis and Yamaguchi, even if possible, requires the signal inversion technique to occur after the D/A converter, allowing for signal decay and introduction of noise. Applicants have found nothing in any of these cited references that teaches or suggests the advantageous feature of Claim 1 discussed above.

II. In any event, there is no motivation to combine the references in the manner set forth in the Office Action.

The Office Action states that

> . . . it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to utilize Yamaguchi's analog signal inversion and Shinya's buffers with Lewis' analog data signals to suppress flicker and crosstalk.

The teaching or suggestion to make the combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143. However, Applicants submit that it would not be possible to combine the technique of inverting and driving analog data lines described Yamaguchi with the techniques of Shinya.

In particular, Yamaguchi teaches inverting and driving analog data lines using alternating current directly from the data drivers to the display screen. In contrast, Shinya does not invert the analog image signals and the display device is driven by a digital signal that enables the output buffers storing the analog image signals. In view of this, incorporating the inversion technique of Yamaguchi would render a combination Lewis, Yamaguchi and Shinya inoperable. Accordingly, there is no reasonable expectation of success.

Furthermore, it is well-settled that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP 2143.01. Shinya teaches the non-inverted analog output of D/A converters are stored by output buffers until a digital output enable signal causes the output buffers to transfer the analog image signals to the data lines simultaneously. However, Yamaguchi teaches that the data signals are driven by alternating current for each data line, so as to be inverted for each data line. Where Shinya incorporates a sample-and-hold circuitry allowing simultaneous feeding to the data lines for one horizontal scanning period permitting, Yamaguchi uses a sequential technique for directly feeding the data lines. The proposed combination of Yamaguchi and Shinya, even

if possible, would require substantial redesign of the elements shown in Shinya as well as a change in the basic principle under which the Shinya construction was designed to operate. Accordingly, that combination is improper.

In addition, even assuming, arguendo, that it would be possible to combine Yamaguchi's polarity inversion technique to Lewis' D/A converter and Shinya's output buffers, the prior art does not suggest the desirability of such a combination. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP 2143.01. While analog signal inversion shown in the background section of Yamaguchi, and relied upon in the Office Action, is described as suppressing flicker and cross talk to some extent, the Yamaguchi reference points out that it is not entirely satisfactory for this purpose since some display patterns may still cause flicker and cross talk.

That is, the technique discussed at col. 2, lines 1-29 is specifically disparaged in Yamaguchi as allowing flicker and cross talk (Column 2, lines 16-29). Thus when Yamaguchi is taken as a whole, it teaches away from seeking to use the conventional techniques discussed at column 2, lines 1-15. In view of this teaching away, the existence of the Yamaguchi reference would not have motivated one of ordinary skill to have made the Examiner's proposed modification to Lewis. On the contrary, Yamaguchi, taken as a whole, would have dissuaded one from making the proposed modification.

Claim 1 is believed clearly patentable over the cited art for at least the reasons discussed above. Claims 18, 38 and 43 also recite similar features discussed above and are believed patentable for at least the reasons developed above with respect to Claim

1. Moreover, the rejections of the independent claims also fails to set forth a *prima facie* case of obviousness for the reasons delineated above.

This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. At the very least, however, entry of this Amendment After Final Rejection, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing remarks, Applicants respectfully request favorable reconsideration.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

18. (Thrice Amended) A liquid crystal device comprising a matrix substrate having plural switching elements provided in matrix corresponding to intersecting points of scanning lines and signal lines, plural picture element electrodes connected to the switching elements, and horizontal circuits and vertical circuits for inputting the signals to the switching elements; a counter substrate opposing to the matrix substrate; and a liquid crystal material placed between the matrix substrate and the counter substrate, the matrix substrate comprising:

a horizontal scanning circuit for sampling a picture data based on digital picture signals;

a latch circuit for memorizing the data synchronously with output from the horizontal scanning circuit;

a D/A converter for converting the output from the latch circuit into analog signals;

plural signal transfer switches provided between D/A converter and the signal lines;

a buffer disposed between said D/A converter and said plural signal transfer switches, which stores the analog signal of inverted polarity from the D/A converter;

a selection circuit for selecting at least one of the signal transfer switches; and

means for inputting signal-polarity inverting signals together with the picture data, and for inverting the polarity of the analog output of the D/A converter,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction.

38. (Twice Amended) A matrix substrate having plural switching elements provided in matrix corresponding to intersecting points of scanning lines and signal lines, plural picture element electrodes connected to the switching elements, a horizontal circuit for inputting the signals to the switching elements, and a vertical circuit for driving said scanning lines, the matrix substrate comprising:

a horizontal scanning circuit for sampling a picture data based on digital picture signals;

a latch circuit for memorizing the data synchronously with output from the horizontal scanning circuit;

a D/A converter for converting the output from the latch circuit into analog signals;

a buffer connected to output of the D/A converter, which stores the analog signal of inverted polarity from the D/A converter; and

polarity inversion means for inputting, together with the picture data, a signal polarity inversion signal and for inverting a polarity of the analog output of said D/A converter according to the signal polarity inversion signal,

wherein a number M of said D/A converters is less than a number N of

said switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction.

43. (Twice Amended) A liquid crystal apparatus, comprising:

a matrix substrate having plural switching elements provided in matrix corresponding to intersecting points of scanning lines and signal lines, plural picture element electrodes connected to the switching elements, a horizontal circuit for inputting the signals to the switching elements, and a vertical circuit for driving the signal lines;

an opposite substrate opposing said matrix substrate; and

a liquid crystal material between said matrix substrate and said opposite substrate,

said apparatus further comprising a horizontal scanning circuit for sampling a picture data based on digital picture signals, a latch circuit for memorizing the data synchronously with output from the horizontal scanning circuit, a D/A converter for converting the output from the latch circuit into analog signals, a buffer connected to the output of the D/A converter, which stores the analog signal of inverted polarity from the D/A converter, and means for inputting a signal polarity inversion signal together with the picture data, and for inverting a polarity of the analog output of said D/A converter according to the signal polarity inversion signal,

wherein a number M of said D/A converters is less than a number N of said switching elements arranged in a horizontal direction, and analog signals are sequentially

inputted from particular ones of said M D/A converters to N/M plural switching elements arranged in a horizontal direction.